AMENDMENTS TO THE CLAIMS:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (currently amended): A multilayered wiring structure for high frequency semiconductor devices, comprising:

a semiconductor substrate;

a ground plate formed above said semiconductor substrate, having a potential fixed at the ground potential;

a plurality of wiring layers, each of which is alternately stacked with an insulating interlayer formed above said semiconductor substrate, the wiring layers combining with said ground plate to form transmission lines; and

at least one separation ~~electrode~~ plate being ~~selectively provided on the additional insulating interlayers~~ stacked between the wiring layers which mutually cross, with insulating interlayers formed therebetween, said at least one separation ~~electrode~~ plate having a potential fixed at the ground potential;,

wherein said at least one separation ~~electrode~~ plate is ~~formed near the~~ selectively provided at a crossing portion where the wiring layers mutually cross~~, with insulating interlayers provided therebetween~~.

Claim 2 (currently amended): A multilayered wiring structure for high frequency semiconductor devices, according to Claim 1, wherein the length and width dimensions of said at least one separation ~~electrode~~ plate are sufficiently smaller than the length of each of the wiring layers used in forming the transmission lines above said semiconductor substrate so as to not significantly interfere with transmission line characteristics of the wiring layers.

Claim 3 (currently amended): A multilayered wiring structure for high frequency semiconductor devices; according to Claim 1, further including additional crossing portions where the wiring layers mutually cross, wherein each of the crossing portions has an individual separation ~~electrode~~ plate.

Claim 4 (currently amended): A multilayered wiring structure for high frequency semiconductor devices; according to Claim 3, wherein the separation ~~electrodes~~ plates are electrically interconnected.

Claim 5 (currently amended): A multilayered wiring structure for high frequency semiconductor devices; according to Claim 3, wherein the separation ~~electrodes~~ plates have a potential which is fixed at the ground potential by one of the wiring layers acting as a common electrode.

Claim 6 (currently amended): A multilayered wiring structure for high frequency semiconductor devices; according to Claim 4, wherein the separation ~~electrodes~~ plates are provided on one of the insulating interlayers, and are electrically interconnected by wiring extended on said insulating interlayer.

Claim 7 (currently amended): A multilayered wiring structure for high frequency semiconductor devices; according to Claim 4, wherein the separation ~~electrodes~~ plates are provided on different insulating interlayers, and are electrically interconnected by at least one through-hole.

Claim 8 (currently amended): A multilayered wiring structure for high frequency semiconductor devices; according to Claim 1, wherein a single separation ~~electrode~~ plate is provided for all of the crossing portions.

Claim 9 (currently amended): A multilayered wiring structure for high frequency semiconductor devices; according to Claim 3, wherein the crossing portions are positioned at different levels, and the separation ~~electrodes~~ plates are provided on those of the insulating interlayers which are provided for all of the crossing portions.

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Claim 10 (currently amended): A multilayered wiring structure for high frequency semiconductor devices, according to Claim 8, wherein the crossing portions are positioned at different levels, and said single separation ~~electrode~~ plate is provided on one of the insulating interlayers which is provided for all of the crossing portions.